Capacitor-less LDO Regulator with High PSR Characteristics

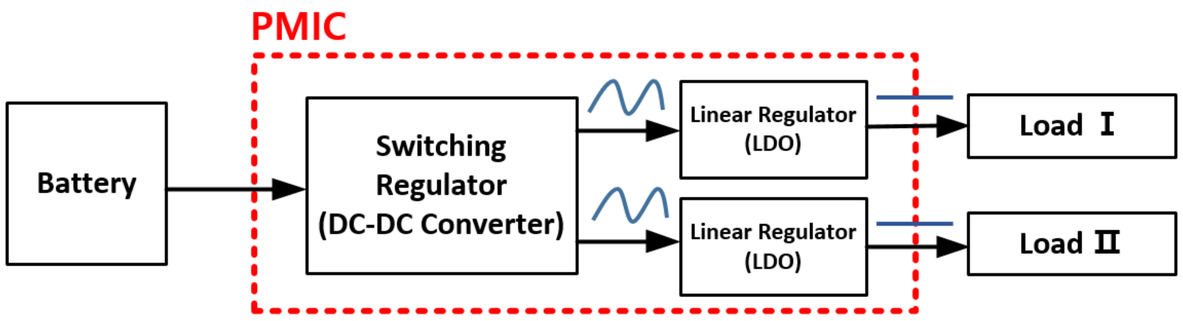
Ung Jae Ra, Jae Rim Baek, Hyunsun Mo, and Daejeong Kim*

Dept. of Electrical Engineering, Kookmin University
Seoul, Korea
tyche@kookmin.ac.kr

Introduction

Power Management Integrated Circuit (PMIC)

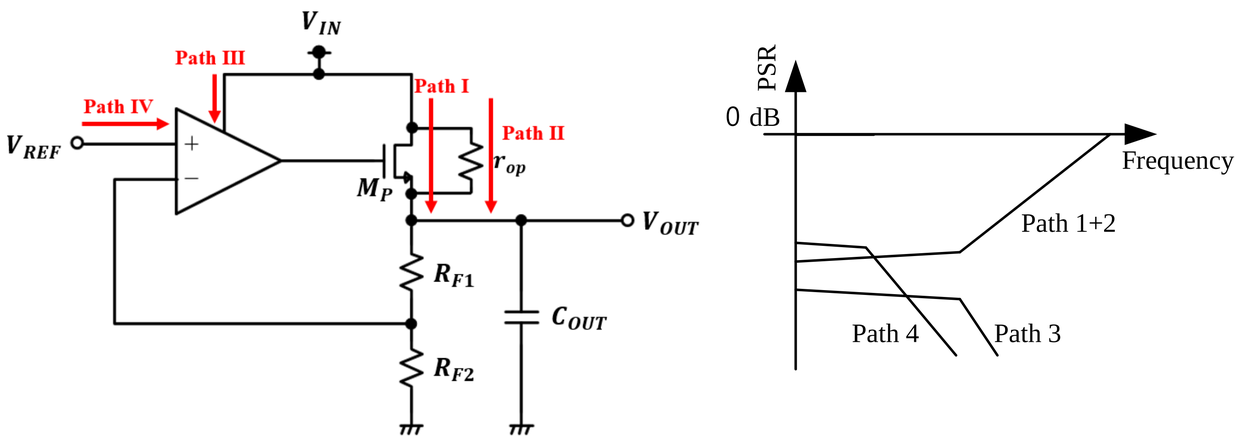
- PMIC is an integrated circuit for power management and contains efficient control and management functions of the battery



Objective

- The switching frequency is increased to reduced the area of the DC-DC switching converter and increase efficiency
- In this paper, we proposed an capacitor-less LDO regulator with wideband PSR characteristic by canceling power supply noise without any hardware overhead or bandwidth limitations of additional analog circuits using High-pass filter and a single compensation transistor

Path that degrade PSR characteristic



Four ripple paths that degrade the PSR characteristic

- Path I : Problem caused by ΔV_{gs} of power MOSFET because the loop bandwidth is not large enough as frequency increases
- Path II : Problem caused by ripple of input voltage transmitted to output node because small signal equivalent resistance(r_{op}) of power MOSFET is finite
- Path III : Problem caused by bandwidth limitation of error amplifier
- Path IV : Problem caused by bandwidth limitation of bandgap reference circuit(BGR)

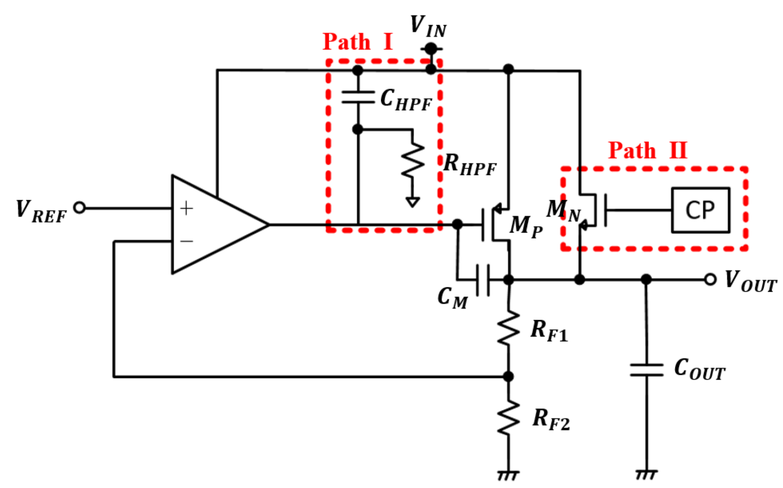
- Path III and Path IV have no effect at high frequency region due to their own bandwidth limitation

- In order to obtain high PSR characteristic in a wide frequency region, it is necessary to solve the problems caused by Path I and Path II together

Acknowledgment

- This work was supported by the IC Design Education Center(IDEC) for the chip fabrication and EDA tool, and it was supported by the Engineering Research Center of MSIP / NRF of Korea Grant funded by the Korean Government(Grant NRF-2016R1A5A1012966 and 2019M3F3A1A02071845)

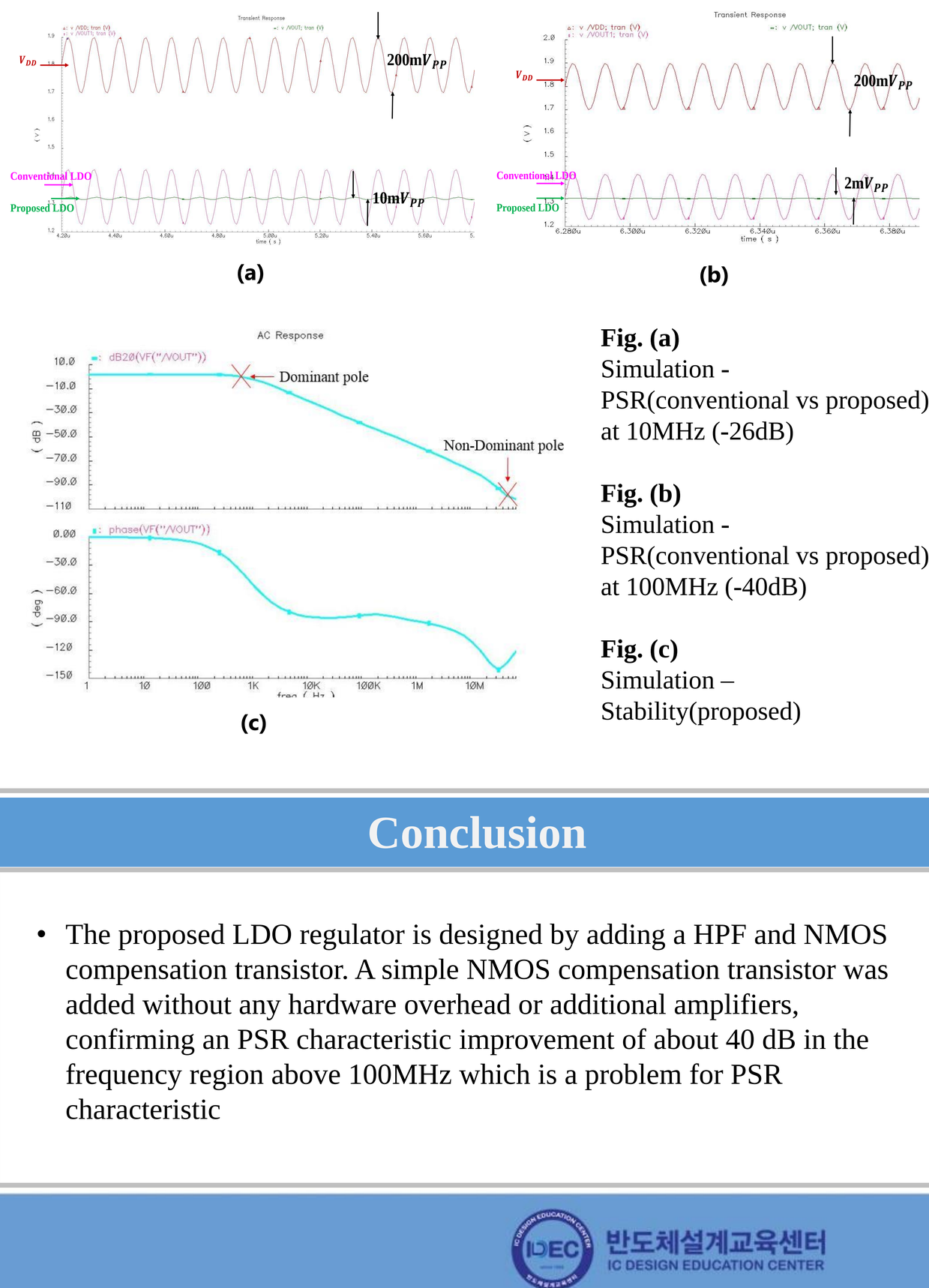
Proposed LDO regulator



Small signal equivalent circuit

- $\frac{v_{in}-v_{out}}{r_{op}} = \frac{v_{out}}{R_1+R_2} + g_{mn}v_{out}$
- $\frac{v_{out}}{v_{in}} = \frac{1}{1+\frac{r_{op}}{R_1+R_2}+g_{mn}r_{op}}$
- $PSR = 20\log\left(\frac{v_{out}}{v_{in}}\right) = -20\log\left(1+\frac{r_{op}}{R_1+R_2}+g_{mn}r_{op}\right)$

Simulation result & Experimental result



(a) (b) (c)

Fig. (a)
Simulation - PSR(conventional vs proposed) at 10MHz (-26dB)

Fig. (b)
Simulation - PSR(conventional vs proposed) at 100MHz (-40dB)

Fig. (c)
Simulation – Stability(proposed)

Conclusion

- The proposed LDO regulator is designed by adding a HPF and NMOS compensation transistor. A simple NMOS compensation transistor was added without any hardware overhead or additional amplifiers, confirming an PSR characteristic improvement of about 40 dB in the frequency region above 100MHz which is a problem for PSR characteristic